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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,863	10/25/2001	Donald Thomas McGrath	RD-27645	9978

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09-682,863	McGrath
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 8-8-2002.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-24 is/are pending in the application.

Of the above claim(s) 6-9 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-5 and 10-24 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCartney 6,380,801 (McCartney) in view of Fujii et al. 5,184,199 (Fujii).

Figures 1 and 5 of McCartney disclose the basic arrangement and method of an operational amplifier employing choppers. A first chopper 102 (16) is placed after an input signal generator and before the input of a first amplifier and a second chopper 26 is placed between the output of the first amplifier and the input of the second amplifier. The amplifiers employ nmos transistors. McCartney fails to disclose the use of silicon carbide nmos depletion mode transistors, however, Fujii clearly points out that such nmos transistors operate under severe conditions like high temperature, high frequency, and radiation exposure and are "expected to have wide applications for devices" (See col. 1, lines 11-26). They are just better transistors compared to pure silicon based transistors.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the nmos transistors of McCartney with silicon carbide nmos depletion transistors so as to enable operation under severe conditions as taught by Fujii.

McCartney also does not disclose the switching elements inside the choppers and the use of silicon carbide nmos depletion transistors for the choppers. Given the advantages of silicon carbide nmos depletion mode transistors as noted above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ such transistors for the chopper so as to take advantage of the operation under severe conditions as taught by Fujii. Note that a device is only as weak as its weakest link and thus it is only common sense to employ better transistors through out a circuit when one wants to operate it in severe conditions.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCarthey and Fujii as applied to claims 1-3 above, and further in view of Richter et al. 4647845 (Richter).

McCartney does not show the details of the device that makes the control signals for the chopper or the use of two nmos silicon carbide depletion transistors for the chopper, however, it is common place to employ as part of the conventional chopper and chopper control circuit two transistors for the chopper and a level shifter in the chopper control circuit so as to ensure that the two switches that must make up a chopper when the signal is applied to two nodes are not on at the same time. Such is shown in Figure 6 and described in column 4 around line 36 of Richter.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the conventional chopper control circuit like that of Richter in McCartney so as to control the two switches in the chopper of McCartney so as to ensure that the two switches are not turned on at the same time as taught by Richter.

Claims 10 and 14-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCartney 6,380,801 (McCartney) in view of Fujii et al. 5,184,199 (Fujii) and Richter et al. 4647845 (Richter).

Figures 1 and 5 of McCartney disclose the basic arrangement and method of an operational amplifier employing choppers. A first chopper 102 (16) is placed after an input signal generator and before the input of a first amplifier and a second chopper 26 is placed between the output of the first amplifier and the input of the second amplifier. The amplifiers employ nmos transistors. McCartney fails to disclose the use of silicon carbide nmos depletion mode transistors, however, Fujii clearly points out that such nmos transistors operate under severe conditions like high temperature, high frequency, and radiation exposure and are "expected to have wide applications for devices" (See col. 1, lines 11-26). They are just better transistors compared to pure silicon based transistors.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the nmos transistors of McCartney with silicon carbide nmos depletion transistors so as to enable operation under severe conditions as taught by Fujii.

McCartney also does not disclose the switching elements inside the choppers and the use of silicon carbide nmos depletion transistors for the choppers. Given the advantages of silicon carbide nmos depletion mode transistors as noted above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ such transistors for the chopper so as to take advantage of the operation under severe conditions as taught by Fujii. Note that a device is only as weak as its weakest

link and thus it is only common sense to employ better transistors through out a circuit when one wants to operate it in severe conditions.

McCartney does not show the details of the device that makes the control signals for the chopper or the use of two nmos silicon carbide depletion transistors for the chopper, however, it is common place to employ as part of the conventional chopper and chopper control circuit two transistors for the chopper and a level shifter in the chopper control circuit so as to ensure that the two switches that must make up a chopper when the signal is applied to two nodes are not on at the same time. Such is shown in Figure 6 and described in column 4 around line 36 of Richter.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the conventional chopper control circuit like that of Richter in McCartney so as to control the two switches in the chopper of McCartney so as to ensure that the two switches are not turned on at the same time as taught by Richter.

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCartney 6,380,801 (McCartney) in view of Fujii et al. 5,184,199 (Fujii) and Richter et al. 4647845 (Richter) as applied to claims 10 and 14-24 above, and further in view of White et al. 4,558,235 (White)

The combination based on McCartney lacks the use of diodes in the level shifter.

Figure 1 White clearly shows the use of diode in the level shifter that forms a load impedance so that the level can be shifted. FETS connected to form a diode are well known art recognized equivalents to that of White.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize FET based diodes in the level shifter so as to from an impedance that enable the level shifting as taught White.

As to the use of resistor loads such are conventional art recognized equivalent loads in a level shifter and as such it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize resistors for the loads in the above McCartney, Fujii, Richter and White combination.

Response to Arguments

Applicant's arguments filed 8-8-2002 have been fully considered but they are not persuasive.

Applicant believes that there is no motivation or suggestion to combine in each of the rejections of the previous Office action. The examiner respectfully disagrees. In the rejection of claims 1-3 involving McCartney and Fujii the motivation is clearly recited and that is Fujii teaches the use of a nmos silicon carbide transistor can operate under high temperature, high frequency and most importantly Fujii teaches that these transistors are to "have wide applications for devices". Fujii himself recognizes that these transistors can be used in many different applications that employ "common" mos transistors. Also applicant argues that there must be some reasonable expectation of success. The examiner has shown a reasonable expectation of success in that the operation of such devices can handle high frequency and still further Fujii believes that these transistors "have wide applications for devices" which clearly indicates that Fujii himself believes there is a reasonable expectation of success with using his transistors in established circuits. Clearly, one of routine skill would have expected that these transistors would work for the frequency range of McCartney. It is noted that Applicant has not shown why one would not have expected the transistors to work in McCartney. Are the results obtained by applicant an unexpected result? In the rejections of claims 4, 5, 10 and 14-24, the examiner has provided able motivation to utilize the chopper of Richter in McCartney and/or Fujii. The chopper of Richter insures that the transistors are not on at the same time that clearly prevents the shorting out of the power supply. One of routine skill would have found it advantageous to employ such a chopper in McCartney for this reason. Furthermore, note that McCarney is silent on the exact structure of the chopper, thereby any conventional chopper circuit could have been used and one or routine skill would have expected success with this. The fact that McCartney discloses more structure that that claimed is immaterial to the rejection. The rejection was

directed to Richter's teaching of an advantageous chopper and not to the placement of the entire structure of Richter in the structure of McCarthney.

Applicant believes that the "prior art teaches away from the present invention" in the rejections. The examiner respectfully disagrees. Applicant in support for this recites the belief that McCartney nor Fujii considered alone or in combination describe or suggest the claimed combination. The examiner respectfully disagreed with this argument above. In addition note that clearly an input signal is generated in McCartney, note the drawing Figures. This signal is amplified using a chopper-stablized operational amplifier as noted above. Again the difference is that McCartney fails to use silicon carbide nmos depletion mode transistors. As noted above there are many advantages known by those of routine skill in the art in using this type of transistors in circuits. One being high output drive (See column 1, line 21 of Fujii). Applicant also believes that this combination does not show the method claimed in claims like claim 22. The examiner respectfully disagrees. The circuit made obvious must provide the method "that includes "amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier". Note that the "complementary" structure shown in McCartney is actually two differential amplifiers that allows for better rail to rail operation whereas applicant's invention is limited in Figure 4 to a only single differential structure. McCartney is clearly composed a many single differential structures. The claims just do not limit the invention to only one differential structure of single conductivity. Furthermore, one of routine skill knows how to utilize enhancement or depletion transistors in a circuit. With respect to the "teaches away from" argument as it relates to claims 4, 5, 10 and 14-24, again applicant argues the no motivation to combine. The examiner respectfully disagrees and directs applicant's attention to the arguments above. Also note that the end result of employing the chopper of Richter includes the buffered logic level shifter and applicant has not argued that it would have been obvious to utilize field effect transistors therein.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Mon-Thurs from 8:30 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
May 1, 2002
October 19, 2002

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817